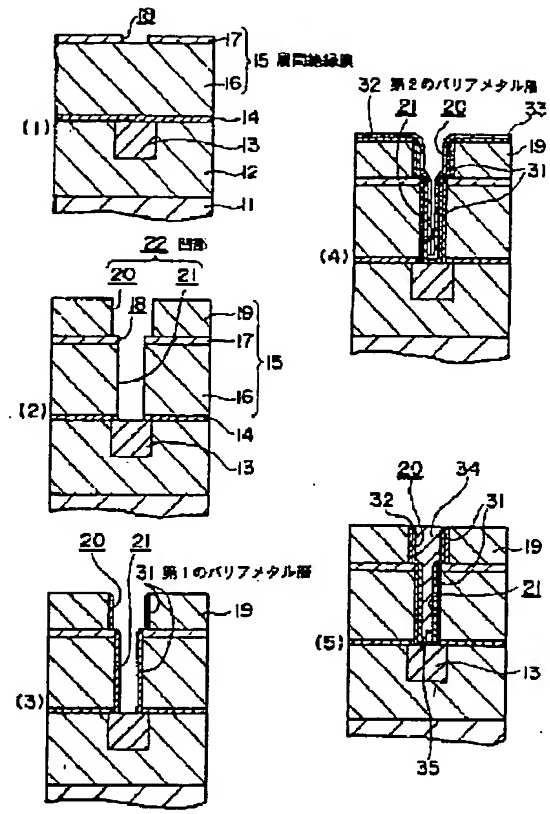
XP-002223600

AN - 2000-685762 [67]
AP - US19980191632 19981113; TW19980114688 19980904
CPY - UNMI-N
DC - L03 U11
FS - CPI;EPI
IC - H01L21/44 ; H01L21/768
IN - HUANG Y; LU H; YOU T; LUR W; YEW T
MC - L04-C13B
- U11-C05D3 U11-C05G2C U11-C07C3 U11-D03B2
PA - (UNMI-N) UNITED MICROELECTRONICS CORP
PN - US6265313 B1 20010724 DW200146 H01L21/44 000pp
- TW389991 A 20000511 DW200067 H01L21/768 000pp
PR - TW19980114688 19980904; US19980191632 19981113
XA - C2000-208506
XIC - H01L-021/44 ; H01L-021/768
XP - N2000-506894
AB - TW389991 NOVELTY - A method for producing a copper interconnect comprises providing a semiconductor substrate formed thereon a dielectric layer having a Cu layer; covering an inter-metal dielectric layer on the dielectric layer; forming a via and a trench opening in the inter-metal dielectric layer to expose the Cu layer; forming a thin barrier layer in the opening and on the Cu layer; bombarding the bottom of the via opening until exposing the surface of Cu metal; filling the via and trench opening with Cu to form a Cu-damascene structure.
- (Dwg.0/0)
IW - METHOD PRODUCE COPPER INTERCONNECT COMPRISE SEMICONDUCTOR SUBSTRATE FORMING DIELECTRIC LAYER COPPER LAYER COVER INTER METAL DIELECTRIC LAYER DIELECTRIC LAYER
IKW - METHOD PRODUCE COPPER INTERCONNECT COMPRISE SEMICONDUCTOR SUBSTRATE FORMING DIELECTRIC LAYER COPPER LAYER COVER INTER METAL DIELECTRIC LAYER DIELECTRIC LAYER
INW - HUANG Y; LU H; YOU T; LUR W; YEW T
NC - 002
OPD - 1998-09-04
ORD - 2000-05-11
PAW - (UNMI-N) UNITED MICROELECTRONICS CORP
TI - Method for producing copper interconnect - comprises providing a semiconductor substrate formed thereon a dielectric layer having a copper layer; covering an inter-metal dielectric layer on the dielectric layer; etc.
USAB- US6265313 NOVELTY - A method for producing a copper interconnect comprises providing a semiconductor substrate formed thereon a dielectric layer having a Cu layer; covering an inter-metal dielectric layer on the dielectric layer; forming a via and a trench opening in the inter-metal dielectric layer to expose the Cu layer; forming a thin barrier layer in the opening and on the Cu layer; bombarding the bottom of the via opening until exposing the surface of Cu metal; filling the via and trench opening with Cu to form a Cu-damascene structure.

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan



PUBLICATION NUMBER : 2000323571

PUBLICATION DATE : 24-11-00

APPLICATION DATE : 14-05-99

APPLICATION NUMBER : 11133532

APPLICANT : SONY CORP;

INVENTOR : TAGUCHI MITSURU;

INT.CL. : H01L 21/768 H01L 21/28 H01L 21/3205

TITLE : MANUFACTURE OF SEMICONDUCTOR DEVICE

ABSTRACT : PROBLEM TO BE SOLVED: To suppress problems such as leakages between wirings caused by the surface of a lower copper wiring being sputtered, where although a natural oxide film on the surface of the lower copper wiring at the bottom of the connection hole can be removed by sputter etching, the sputtered copper adheres to the sidewall of a connection hole and the stuck copper shifts within an interlayer insulating film, and others.

SOLUTION: This manufacturing method is equipped with a process of forming a recess 22 consisting of a groove 20 and a connection hole 22 in an interlayer insulating film 15, a process of forming a first barrier metal layer 31 at the inner face of the recess 22, a process of exposing the bottom of the recess 22, by selectively removing the first barrier metal layer 31 at the bottom of the recess 22, a process of performing sputter etching to the bottom of the recess 22, and a process of forming a second barrier metal layer 31 via the first barrier metal layer 31 at the inner face of the recess 22.